In The Claims:

Claim 1 (currently amended) An apparatus for supporting multi-processors, wherein said apparatus is coupled to a central processing unit (CPU) socket, having a plurality of connecting pins, and when said CPU socket is inserted with a first type CPU, a first pin among said connecting pins has a first equivalent resistance, and when said CPU socket is inserted with a second type CPU, said ~~second~~ first pins has a second equivalent resistance, wherein the first equivalent resistance is not equal to the second equivalent resistance, said apparatus comprising:

a distinguish device, coupled to said first pin to ~~apply a~~ use difference between said first and said second equivalent resistances to generate a CPU select signal; and

a switch circuit, coupled to said distinguish device and said CPU socket to selectively connect a plurality of first type CPU signals to said corresponding connecting pins, and a plurality of second type CPU signals to said corresponding connecting pins according to ~~control a~~ status of said CPU select signal.

Claim 2 (currently amended) The apparatus according to claim 1, wherein when said CPU socket is inserted with said first type CPU, a second pin among said connecting pins has a third equivalent resistance, and when said CPU socket is inserted with said second type CPU, said second pin has a fourth equivalent resistance, wherein the third equivalent resistance is not equal to the fourth equivalent resistance, and said distinguish device is coupled to said second pin to use a difference between said first, second, third and said fourth equivalent resistance to determine a type of said CPU inserted in said CPU socket, and to generate a CPU select signal.

Claim 3 (currently amended) The apparatus according to claim 2, wherein said apparatus further receives a suspend status input signal, and said distinguish device further comprises:

a processor select circuit, coupled to said first and said second pins to use a difference between said first, said second, said third and said fourth equivalent resistances to generate a CPU select signal; and

an interval control circuit, to receive said suspend status input signal and delay said suspend status input signal with a predetermined stop determination time, so that said processor select circuit cuts off ~~said~~ a connection between said first pin and said processor select circuit.

Claim 4 (original) The apparatus according to claim 3, wherein said interval control circuit comprises:

a first delay circuit, receiving and delaying said suspend status input signal with said predetermined stop determination time to generate a cutoff activating signal; and

a second delay circuit, coupled to said first delay circuit to receive said cutoff activating signal and to generate a suspend status output signal after delaying a predetermined buffer time; wherein

said interval control circuit enable said processor select circuit to cut off a connection between said processor select circuit and said first and second pins, and a computer system that comprises said apparatus outputs a signal to activate according to said suspend status output signal.

Claim 5 (original) The apparatus according to claim 4, wherein said interval control circuit further comprises:

a first resistor, with a first end coupled to a fixed voltage and a second end; and

a latch circuit, with an input terminal, an output terminal and a control terminal, wherein said control terminal is coupled to said first delay device and said input terminal is coupled to said second end of said first resistor to receive a control of said cutoff activating signal and outputs a cutoff latch signal.

Claim 6 (currently amended) The apparatus according to claim 3, wherein said processor select circuit comprises:

a first switch transistor, with a first terminal, a second terminal and a control terminal, wherein said first terminal is coupled to said first pin, said control terminal is coupled to said interval control circuit to either cutoff or conduct said connection between said first pin and said processor select circuit selects;

a second resistor, with a first end coupled to said second terminal of said first switch transistor and a second end;

a first constant current source, coupled to said second end of said second resistor to provide a first constant current;

a second constant current source, to provide a second constant current, wherein a difference between said first and said second constant currents is smaller than a predetermined value;

a third resistor, with a first end and a second end coupled to said second constant current source;

a fourth resistor, with a first end coupled to a first fixed potential and a second end coupled to said first end of said second resistor;

a fifth resistor, with a first end coupled to said first fixed potential and a second end coupled to said first end of said third resistor, wherein said fourth resistor has a resistance different from that of said ~~fourth~~ fifth resistor; and

a first operation amplifier, with a first input terminal, a second input terminal and an output terminal, wherein said first input terminal is coupled to said first end of said second resistor, said second input terminal is coupled to said first end of said third resistor, and said output terminal outputs a first type signal.

Claim 7 (original) The apparatus according to claim 6, wherein said processor select circuit comprising:

a second switch transistor, comprising a first terminal, a second terminal and a control terminal, wherein said first terminal is coupled to said second pin, said control terminal is coupled to said interval control circuit to either cut off or conduct a connection between said second pin and said processor select circuit;

a sixth resistor, with a first end and a second end coupled to a second fixed potential;

a third switch transistor, comprising a first terminal, a second terminal and a control terminal, wherein said first terminal is coupled to said second pin, said second terminal is coupled to said first end of said sixth resistor, and said control terminal is coupled to said interval

control circuit to cut off or conduct a connection between said second pin and said sixth resistor; and

a second operation amplifier, comprising a first input terminal, a second input terminal and an output terminal, wherein said first input terminal is coupled to said second terminal of said second switch transistor, said second terminal is coupled to a third fixed potential, and said output terminal is coupled to a second type signal.

Claim 8 (original) The apparatus according to claim 7, wherein said processor select circuit further comprises a logic circuit to receive said first type signal and said second type signal to generate said CPU select signal.

Claim 9 (currently amended) The apparatus according to claim 1, further receiving a suspend status input signal, wherein said distinguish device further comprises:

a processor select circuit, coupled to said first pin to use a difference between said first equivalent resistance and said second equivalent resistance to generate said CPU select signal; and

an interval control circuit, to receive and delay said suspend status input signal with a predetermined stop determination time, so that said processor select circuit cuts off a connection between said first and second pin and said processor select circuit.

Claim 10 (original) The apparatus according to claim 9, wherein said interval control circuit comprising:

a first delay circuit, to receive and delay said suspend status input signal with a predetermined stop determination time to generate a cutoff activating signal; and

a second delay circuit, coupled to said first delay device to generate a suspend status output signal after receiving and delaying said cutoff activating signal with a predetermined buffer time;

wherein said interval control circuit cuts off a connection between said first pin and said processor select circuit according to said cutoff activating signal, and a computer system comprising said apparatus is activated according to said suspend status output signal.

Claim 11 (original) The apparatus according to claim 9, further coupled to a power regulator that provides a correct source voltage to said CPU inserted in said CPU socket according to said suspend status output signal and said CPU select signal.

Claim 12 (original) The apparatus according to claim 9, wherein said processor select circuit comprises an activate determination control circuit that enable said processor select circuit to operate after receiving said suspend status input signal, so as to determine said type of said CPU inserted in said CPU socket.

Claim 13 (original) The apparatus according to claim 1, wherein said distinguish device is supplied power from a prepared power supply.

Claim 14 (original) A method for supporting multi-processors in a single motherboard, applied to a computer system that comprises a CPU socket and a suspend status input signal, wherein the CPU socket comprises a plurality of connecting pins of which a first pin has a first

equivalent resistance when a first type CPU is inserted in said CPU socket, and has a second resistance when said CPU socket is inserted with a second type CPU, said method comprising:

using a difference between said first equivalent resistance and said second equivalent resistance to generate a CPU select signal; and

selectively connecting a plurality of first CPU signals to said corresponding connecting pins, and a plurality of second type CPU signals to said corresponding pins according to said CPU select signal.

Claim 15 (currently amended) The method according to claim 14, further comprising a ~~said~~ step of delaying said suspend status input signal with a predetermined stop determination time after receiving, and determining which type of said CPU is inserted in said CPU socket within said predetermined stop determination time.

Claim 16 (original) The method according to claim 14, further comprising the step of further delaying the suspend status input signal with a predetermined buffer time after the predetermined stop determination time to allow said CPU is inserted in said CPU socket operating normally.

Claim 17 (original) The method according to claim 14, wherein a second pin among said connecting pins has a third equivalent resistance when said first type CPU is inserted in said CPU, and has a fourth equivalent resistance when said second type CPU is inserted in said CPU, and a difference between said third equivalent resistance and said fourth equivalent resistance is used to determined said type of said CPU inserted in said CPU socket.